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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,302	11/14/2003	Andrew H. Barr	200308580-1	2112

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EXAMINER	
MCCARTHY, CHRISTOPHER S	
ART UNIT	PAPER NUMBER
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,302	BARR ET AL.	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *response to arguments*.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-3, 5-14 of U.S. Patent Application #10/714,386 contain every element of claims 1-3, 6-14 of the instant application and as such anticipates claims 1-3, 6-14 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adamane et al. U.S. Patent Application Publication US2003/0115385A1 in view of *Microsoft Computer Dictionary* (Microsoft).

As per claim 1, Adamane teaches a computer system comprising: a processor (fig. 1, 101); a first bus coupled to the processor (fig.1, 102); a memory (fig. 1, 104,108); a core electronics complex (figure 1, wherein the entire figure and its contents make up the core components of the system); a first input/output (I/O) controller coupled to the first bus (fig. 1, 118; fig.2, 202; ¶ 0015); and a test module coupled to the first I/O controller (¶ 0015, 0021); wherein the test module is configured to cause tests to be performed on the memory using the first bus (¶ 0021). Adamane does not explicitly teach a memory coupled to the memory controller and, therefore, a memory controller coupled to the first bus and memory. Microsoft teaches a memory controller (page 112, in the definition of a control unit). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory controller of Microsoft in the memory system of Adamane. It would have been obvious to one of ordinary skill in the art to use the memory controller of Microsoft in the memory system of Adamane because Microsoft teaches the controller to control access to the unit; this is an explicit desire of Adamane (¶ 0015).

As per claim 2, Adamane teaches the computer system of claim 1 further comprising: an operating system (¶ 0011, 0013, wherein, Adamane teaches the processing system to be running a set of instructions/program that imparts functionality to the system, in light of the taught system having software that controls devices such as memories, and I/O devices, the examiner contends that this functional program is an operating system, according to the Microsoft Computer Dictionary definition of a n operating system (page 321)); wherein the processor is configured to cause the operating system to be booted (¶ 0011, wherein, if the processor runs the functional program, it must have started/booted the operating system at an earlier time), and wherein the test module is configured to cause the tests to be performed on the memory using the first bus subsequent to the operating system being booted (¶ 0015, wherein, the operating system must be running/been booted to operate the system).

As per claim 3, Adamane teaches the computer system of claim 1 further comprising: an operating system (¶ 0011, 0013, wherein, Adamane teaches the processing system to be running a set of instructions/program that imparts functionality to the system, in light of the taught system having software that controls devices such as memories, and I/O devices, the examiner contends that this functional program is an operating system, according to the Microsoft Computer Dictionary (page 321)); wherein the processor is configured to cause the operating system to be executed (¶ 0011), and wherein the test module is configured to cause the tests to be performed on the memory using the first bus during execution of the operating system (¶ 0015, wherein, the operating system must be running/been booted to operate the system).

As per claim 4, Adamane teaches the computer system of claim 1 wherein the first bus comprises a system bus (fig. 1, 102).

As per claim 5, Adamane teaches the computer system of claim 1 further comprising: a second bus (fig.1, 116); and a device coupled to the second bus (fig. 1, 118); wherein the core electronics complex includes a second I/O controller coupled to the first bus (fig. 1, 118; fig. 2, 202) and the second bus (fig 1, 116).

As per claim 6, Adamane teaches the computer system of claim 1 wherein the test module is configured to cause tests to be performed on the memory using the first bus by providing read and write transactions to the first I/O controller (¶ 0021).

As per claim 7, Adamane teaches the computer system of claim 6 wherein the read and write transactions comprise direct memory access (DMA) transactions (¶ 0015, 0021).

As per claim 8, Adamane teaches the computer system of claim 1 further comprising: a bus bridge coupled to the first bus and the first I/O controller (fig. 1, 110).

As per claim 9, Adamane teaches a method performed by a computer system that includes a memory comprising: selecting a portion of the memory for testing during operation of the computer system (¶ 0015, wherein a portion of memory can be said to be the cache of the memory system as a whole); generating a test transaction in a test module coupled to an input/output (I/O) controller (¶ 0015, 0022), the test module and the I/O controller included in a a chipset coupled to the memory (fig. 1); and providing the test transaction to the portion using direct memory access (DMA) (¶ 0015, 0022).

As per claim 10, Adamane teaches the method of claim 9 further comprising: detecting an error that occurs in response to the test transaction (¶ 0022, wherein, false sharing is indicative of an invalid action); and performing a remedial action in response to detecting the error (¶ 0015, wherein, the results are stored and further analyzed to observe the effects of the action).

As per claim 11, Adamane teaches the method of claim 9 further comprising: providing the test transaction from the test module to the I/O controller (¶ 0015, 0022); providing the test transaction from the I/O controller to a bus bridge included in the chipset (fig. 1); providing the test transaction from the bus bridge to a system bus (fig. 1); providing the test transaction from the system bus to a memory (fig. 1); and providing the test transaction from the memory controller to the portion (fig. 1; ¶ 0015). Adamane does not explicitly teach a memory controller. Microsoft teaches a memory controller (page 112, in the definition of a control unit). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory controller of Microsoft in the memory system of Adamane. It would have been obvious to one of ordinary skill in the art to use the memory controller of Microsoft in the memory system of Adamane because Microsoft teaches the controller to control access to the unit; this is an explicit desire of Adamane (¶ 0015).

As per claim 12, Adamane teaches the method of claim 11 further comprising: storing information in the memory in response to the test transaction being a write transaction (¶ 0015).

As per claim 13, Adamane teaches the method of claim 11 further comprising: in response to the test transaction being a read transaction (¶ 0015, 0021): providing information associated with the test transaction from the portion to the memory (fig. 1); providing the information from the memory to the system bus (fig. 1); providing the information from the system bus to the bus bridge (fig. 1); providing the information from the bus bridge to the I/O controller (fig. 1; fig. 2); and providing the information from the I/O controller to the test module (fig. 2). Adamane does not explicitly teach a memory controller. Microsoft teaches a memory controller (page 112, in the definition of a control unit). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to use the memory controller of Microsoft in the memory system of Adamane. It would have been obvious to one of ordinary skill in the art to use the memory controller of Microsoft in the memory system of Adamane because Microsoft teaches the controller to control access to the unit; this is an explicit desire of Adamane (¶ 0015).

As per claim 14, Adamane teaches the method of claim 9 further comprising: providing the test transaction from the test module to the I/O controller (fig. 2); providing the test transaction from the I/O controller to a system controller included in the chipset (fig. 1); providing the test transaction from the system controller to a memory (fig. 1); and providing the test transaction from the memory controller to the portion (fig. 1; ¶ 0015, 0021). Adamane does not explicitly teach a memory controller. Microsoft teaches a memory controller (page 112, in the definition of a control unit). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory controller of Microsoft in the memory system of Adamane. It would have been obvious to one of ordinary skill in the art to use the memory controller of Microsoft in the memory system of Adamane because Microsoft teaches the controller to control access to the unit; this is an explicit desire of Adamane (¶ 0015).

As per claim 15, Adamane teaches a computer system comprising: a processor (fig. 1); a bus coupled to the processor (fig. 1); a core electronics complex (fig. 1) including: an input /output (I/O) controller (fig. 2); and a test module coupled to the I/O controller (fig. 2); wherein the test module is configured to cause tests to be performed on the memory using direct memory access (DMA) (fig. 2; ¶ 0015). Adamane does not explicitly teach a system controller and all the claimed couplings to the system thereof, but does teach a memory (fig. 1). Microsoft teaches a

system controller in the form of a memory controller (page 112, in the definition of a control unit). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory controller of Microsoft in the memory system of Adamane. It would have been obvious to one of ordinary skill in the art to use the memory controller of Microsoft in the memory system of Adamane because Microsoft teaches the controller to control access to the unit; this is an explicit desire of Adamane (¶ 0015).

As per claim 16, Adamane teaches the computer system of claim 15 further comprising: an operating system (¶ 0011, 0013, wherein, Adamane teaches the processing system to be running a set of instructions/program that imparts functionality to the system, in light of the taught system having software that controls devices such as memories, and I/O devices, the examiner contends that this functional program is an operating system, according to the Microsoft Computer Dictionary (page 321)); wherein the processor is configured to cause the operating system to be booted (¶ 0011, wherein, if the processor runs the functional program, it must have started/booted the operating system at an earlier time), and wherein the test module is configured to cause the tests to be performed on the memory using DMA subsequent to the operating system being booted (¶ 0015, wherein, the operating system must be running/been booted to operate the system).

As per claim 17, Adamane teaches the computer system of claim 15 further comprising: an operating system (¶ 0011, 0013, wherein, Adamane teaches the processing system to be running a set of instructions/program that imparts functionality to the system, in light of the taught system having software that controls devices such as memories, and I/O devices, the examiner contends that this functional program is an operating system, according to the

Microsoft Computer Dictionary (page 321)); wherein the processor is configured to cause the operating system to be executed (¶ 0011), and wherein the test module is configured to cause the tests to be performed on the memory using DMA during execution of the operating system (¶ 0015, wherein, the operating system must be running/been booted to operate the system).

As per claim 18, Adamane teaches the computer system of claim 15 wherein the bus comprises a system bus (fig. 1, 102).

As per claim 19, Adamane teaches the computer system of claim 15 wherein the test module is configured to cause tests to be performed on the memory using DMA by providing read and write transactions to the I/O controller (¶ 0021).

As per claim 20, Adamane teaches the computer system of claim 19 wherein the read and write transactions comprise direct memory access (DMA) transactions (¶ 0015, 0021).

Response to Arguments

4. Applicant's arguments filed 11/3/06 have been fully considered but they are not persuasive.

The applicant has argued and amended the claims to include new language that is present in the specification. The examiner will address these new limitations below.

As per claims 1, 5, and 15, the applicant has amended the claim to include the language of "a core electronics complex including:" and has argued that this overcomes the applicable rejected claims. The examiner respectfully disagrees. Using the Webster's Dictionary definition of a complex as consisting various parts; along with the term core as a central part; the examiner

interprets the new language to mean various electronic parts making up a central part of the computer system. The examiner contends that the Adamane reference teaches this in figure 1 as the entire figure represents various electronic parts that make up the central part of the computer system.

As per claims 9, 11, and 14, the applicant has amended the claims to include language of a chipset and has argued that this overcomes the applicable rejections. The examiner respectfully disagrees. Using the definition of a chipset given my the Microsoft Computer Dictionary as a collection of chips designed to function as a unit in a task; the examiner contends that the rejections, as cited, teach this inherent limitation; that is, the system of figure 1 of Adamane comprises multiple chips (in at least the forms of controllers, which are processors and are chips by definition) to perform the desired function, and, therefore, teaches the new language. If the applicant wishes to further limit the existing to where the test module and the I/O controller are the only chips in the chipset, then the applicant is urged to put that into claim language.

Furthermore, the double patenting rejection is maintained as the new language does not differentiate the language to overcome the co-pending application; in that, drawing a box around existing objects (as in the language of a core electronic complex or a chipset) that are the same objects as the co-pending application, without the box, does not take away that the same objects still exist.

In light of the above arguments, all applicable rejections stand.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

csm